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Implementation of built in self test (BIST) enabled UART using FPGA for fault detection

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Abstract
This paper primarily focus on the examination of error that incorporated in datum during its transmission over the communication link. Thus, for improving steadiness and the quickness of error detection of data, it is needed to embed the examining property within the universal asynchronous receive/transmit (UART) chip. Implementation starts with the designing of basic UART module, multiple input signature register (MISR) and a comparator/tester individually using Verilog HDL. The whole design is now, assembled and upgrade for minimal on chip area with fast speed, simulated on Isim simulator, incorporate and checked on field programmable gate array (FPGA) to authenticate the design.

Keywords: UART, MISR, FPGA, HDL

1. Introduction
Interfacing using UART is performed on a specific baud rate along with the sampling to obtain competent link between different peripherals. A UART is an IC which shows a crucial role in linking the synchronous peripherals with the asynchronous peripherals by building the communication procedure between them. It primarily controls the reorganization of serial and parallel data [1]. The MISR is modeled for the sharing of signature bits with the data bits over the same link. This makes error analysis simple and checks any delay faults [3].

2. Verilog implementation
With the advancement in integrated circuit technology, it has become very tedious and time consuming to design systems at basic building element level to flip flop level. In such reference the use of HDL in the development of digital design has notably enhanced in the latest years, exclusively for FPGA architecture. Verilog HDL allows designer to design a digital system and debug at a higher level before changeover to the basic building element level to flip flop level [6]. Verilog is one such suitable HDL which allows characterizing and simulating the activity of an array of digital systems, differing from complexity of a basic building element to an interconnection of any complicated ICs.

3. UART with MISR register and tester
Before using for communication, the clear to receive (ctr) pin of UART depicted in Fig.2 has to link with the clear to send (cts) pin to provide the handshaking signal and the (serial out) pin with the (serial in) pin for the datum. Reset is an active high pin and hence it is required to put at low logic level for UART to keep working. Data can be write at (parallel in) pin by setting (write) pin at high logic for at least of one clock cycle. MISR mode can be activate by setting the (mode) pin at high logic level.
In the modeling of UART, MISR is helps in the formation of signature bits. MISR architecture has D flip-flops with the XOR gates in feedback. Number of flip-flops decides the word size of signature.

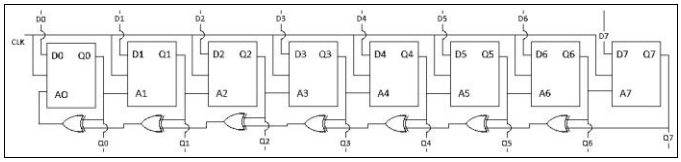

Fig 1: 8 stage MISR.

MISR depicted above produces an 8-bits signature. The signature is transmitted after the data frame. The frame received contains both data and signature, the data is fed to the (MISR RX) block to develop the signature again for comparison with the signature received on the communication link. Dissimilarity of signature sets up an (error) signal.

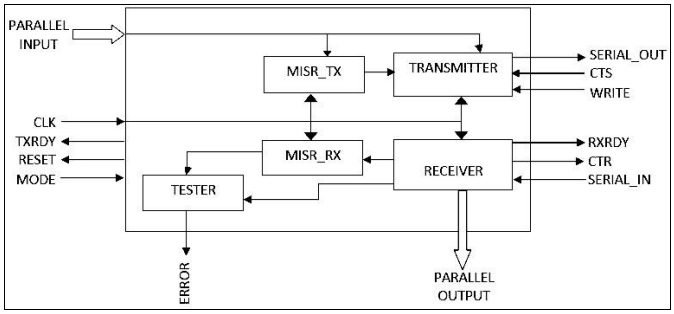

Fig 2: UART block digram.

4. Simulation
For normal working (mode) pin will given a low logic. The transmitter and receiver working under normal operation as shown in Fig.3 will be determined next. The operation of UART in fault detection mode as shown in Fig.6 is shown in the next section.

A. UART normal mode

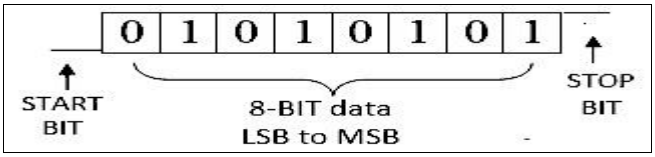

Fig 3: Normal mode frame.

1. Transmitter simulation: The waveform shown in fig.4 shows the transmission procedure of UART. Data bits are arranged between the start and stop bit as shown in fig.3. Start bit, is at low logic level for the time period of the baud rate. Start bit is trailed by data frame from LSB to MSB. After the transmission of data frame, Stop bit is transmitted which put the line on high logic level untill next start bit arrives.

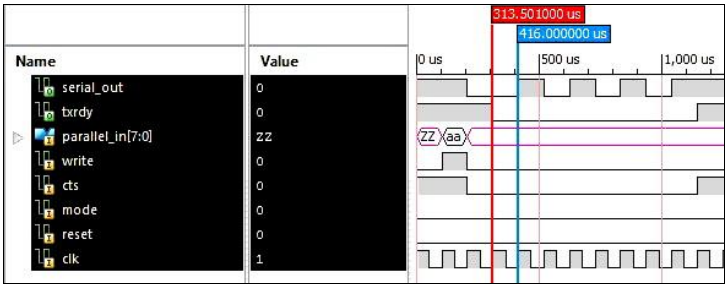

Fig 4: Serial data transmission in normal mode.

It is examined from the above waveform shown in fig.4 that, when (parallel in) is AAH, the sequence of "01010101" data will be show up on (serial out). The duration of each data bit is equal to 104.167µs. From this guidance, the bit rate can be determined as 9600bps.

2. Receiver simulation: 8-bit serial data with start and stop bit is received at the (serial in) pin as shown in Fig 5. The serial data is now changed back into the parallel data to make it available at (parallel out) pin.

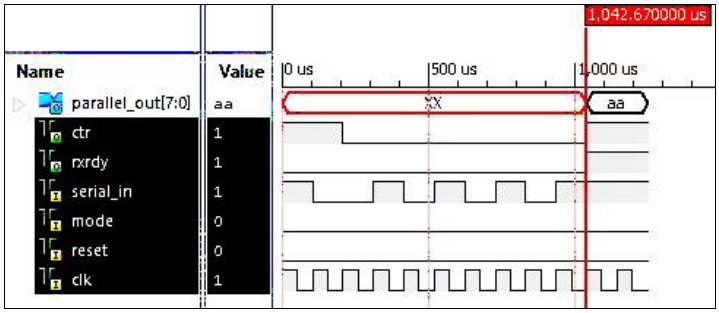

Fig 5: Serial data reception in normal mode

Prior to the arrival of start bit as shown in fig.5, the receiver will remain in ideal state and it is waiting for (serial in) to make a transition from high to low logic level, which is indicated as a start of frame. Once a Start bit is encountered, data bit is stored into the receiver store register.

B. UART in MISR mode

In this error detection mode, the (mode) pin will be put at high logic level to set the UART in BIST operation mode. It takes 5-clock cycles to generate signature frame.

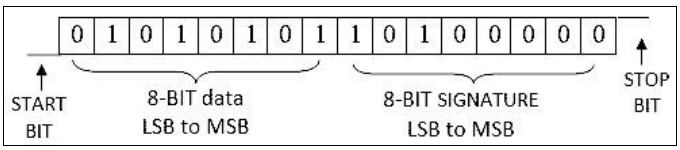

Fig 6: MISR mode frame.

1. Transmitter simulation: The waveform displayed in fig.7 shows the transmission of a 16-bit frame at the (serial out) pin, in which 8-bits are reserved for data and 8-bits for signature illustrated in fig.6.

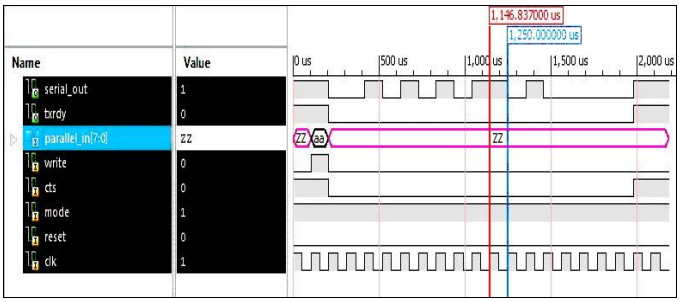

Fig 7: Serial data transmission in MISR mode.

It is noticed from the waveform in fig.7, that during (parallel in) is AAH, the frame of "0101010110100000" will appear on (serial out). The signature bits follows the data bits as shown in fig.6.

2. Receiver simulation: Simulation of fig.8 shows that if the received frame is same as transmitted frame, the (error) pin is low and the data is considered as error free.

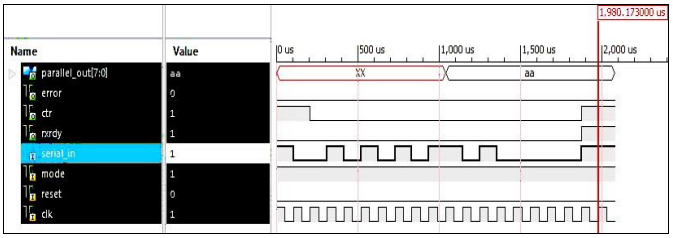

Fig 8: Serial data reception in MISR mode with no error.

The Simulation in fig.9 shows that if the received frame is different from the transmitted frame, the (error) pin is high and the data is considered as faulty.

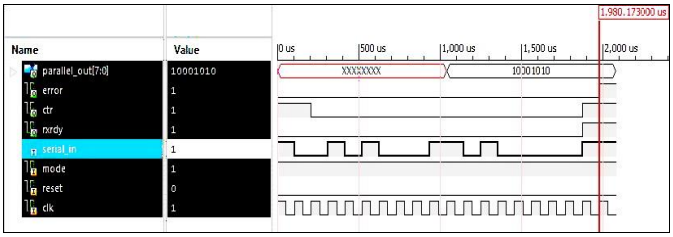

Fig 9: Serial data reception in MISR mode with error.

5. UART description

A. Pin description

Table 1: UART pin description

Pin	In/Out	Description
Parallel in	In	Parallel input from CPU.
Parallel out	Out	Parallel output to CPU.
Serial in	In	Serial input at receiver module.
Serial out	Out	Serial output at transmitter module.
Clk	In	Clock
Reset	In	Clears all control logic and registers when input is high.
mode	In	Mode selection '1'= UART is in MISR mode. '0' = UART is in normal mode.
Error	Out	Error in received signal
Txrdy	Out	Transmitter ready Transmitter is ready to take parallel data frame as input when this output pin is high.
Rxrdy	Out	Receiver ready Receiver is ready to read parallel data frame when this output pin is high.
Cts	In	Clear to send Transmitter is allowed to send serial data over line if this input pin is high.
Ctr	Out	Clear to receive Receiver is ready to receive serial data over line if this output pin is high.

B. Device utilization summary

The whole UART with BIST compatibility is implemented with efficient area and gates utilization.

The comparison of UART implementation with embedded BIST architecture on the basis of delay and area overhead is shown in table II. It was observed that area overhead after the implementation of MISR is reduced from 190 to 93 and net delay is reduced from 13.626ns to 5.688ns in comparison with previously implemented BIST technique [2].

Table 2: Comparison of area overhead

Logic Utilization	Uart	Uart misr	Uart bist
Number of slices (4656)	45	93	190
Number of slice flip flops (9312)	37	100	158
Number of 4 input LUTs (9312)	69	176	342
Number of bonded IOBs (232)	25	27	35
Number of GCLKs (24)	1	1	1
Maximum net delay (ns)	5.376	5.688	13.626

6. Conclusion

The simulated waveforms confirms the speed and accuracy UART with BIST architecture, implemented on FPGA using Verilog HDL. The test is simulated at a bit rate of 9600bps. The UART module takes advantage of nearly 100% fault coverage which is the most crucial thing in any design to ensure the reliability by their designer of their design. The consequent objective for this experimentation is to employ the memory for storing more than 1-frame of data and an internal clock mechanism.

7. References

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