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# Analysis and effects of changes in supply voltage on performance parameter of inverter based 10-stage delay line

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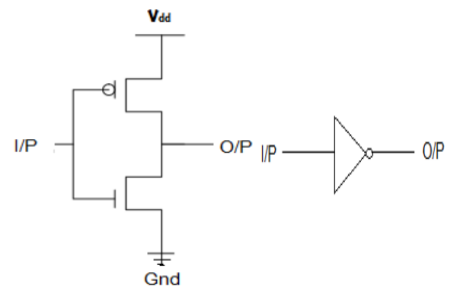
**Abstract**
As per the today requirement, variation in fixed parameter should not effect on performance parameters like propagation delay, leakage current, leakage power and power delay product (PDP). So this article focused on the effects of changes in supply voltage (0.5V- 1.5V) on the various performance parameter of 10-stages inverter based delay line based on CMOS architecture. A delay line is a discrete element in digital theory, which simply allows a signal to be delay by the number of samples. The effects of changes in supply voltage on leakage current, leakage power, propagation delay and PDP product has been studied in this article. Spice simulation tool is used for this analysis with 45nm technology node.

**Keywords:** supply voltage, leakage power, leakage current, power delay product, propagation delay

## 1. Introduction
Delay line is devices that introduced time delay to signals by a pre-determined time constant. Delay line play a substantial role in many sub-system of time interval measurement circuit such as time to digital converter and digital to time converter for the digitization of short time interval.
CMOS delay lines are used in the applications of the clock distribution and clock data recovery (CDR) to satisfy the growing need for precise clock deskew and inaccurate pulse-edge placement control for testing and debugging the dynamic behavior of high speed and high performance digital VLSI circuit. Delay line based analog to digital converter [3], single stage vernier time to digital converter [4]
This delay line generating by connecting inverters because the inverter is usually accepted doing Boolean operation. The inverter is usually accepted as the most basic logic gate doing Boolean operation on a single input variable fig.1 shows the symbol truth table and a general structure of a CMOS inverter.




(A) (B)

| I/P | O/P |
|---|---|
| 0 | 1 |
| 1 | 0 |

(c)

**Fig 1: (a)** general structure **(b)** symbol **(c)** truth table of inverter

## 2. Switching Threshold
The switching threshold, $V_M$, *is defined as the point where* VIN = Vout. Its value can be obtained graphically from the intersection of the VTC with the line given by VIN = Vout (see Fig2). In this figure the cut point between both the lines shows the switching threshold voltage point. Here switching threshold is equal to the half of supply voltage. In this region, both PMOS and NMOS are always saturated, since $V_{DS} = V_{GS}$. An analytical expression for $V_M$ is obtained by equating the currents through the transistors. Here we bypass the derivation for switching threshold voltage. Equation of switching threshold for inverter will be [2],

$$V_{th}(INR) = \frac{V_{T,n} + \sqrt{\frac{k_p}{k_n}}(V_{DD} - |V_{T,p}|)}{1 + \sqrt{\frac{k_p}{k_n}}}$$

By the above equations we can easily say, that switching threshold is depend on the supply voltage and transistor width ratio fig.2. This figures shows how switching threshold affected by changing the value of supply voltage and transistor. We can easily say that by increasing the supply voltage our switching threshold voltage will be shifted for inverter. This is also proved by the simulated results as shown in figure1. Switching threshold is also depending on the width of NMOS and PMOS transistor as shown in fig.2. By increasing the width of PMOS, switching threshold moved towards the supply voltage and by increasing the width of NMOS transistor, switching threshold moved towards the ground [1]. In which full derivation for this expression are given for better understanding. But it is not necessary to make our device symmetric; there are many applications where symmetric property are not applied. And it is also possible to make our circuit faster in non-symmetric devices [1].

So far, we have consistently widened the PMOS transistor so that its resistance matches that of the pull-down NMOS device. This typically requires a ratio of 3 to 3.5 between PMOS and NMOS width. The motivation behind this approach is to create an inverter with a symmetrical VTC, and to equate the high-to-low and low-to-high propagation delays. However, this does not imply that this ratio also yields the minimum overall propagation delay. If symmetry and reduced noise margins are not of prime concern, it is actually possible to speed up the inverter by reducing the width of the PMOS device! [1].

The reasoning behind this statement is that, while widening the PMOS improves the $\tau_{PLH}$ of the inverter by increasing the charging current, it also degrades the $\tau_{PHL}$ by cause of a larger parasitic capacitance. When two contradictory effects are present, there must exist transistor ratio that optimizes the propagation delay of the inverter.

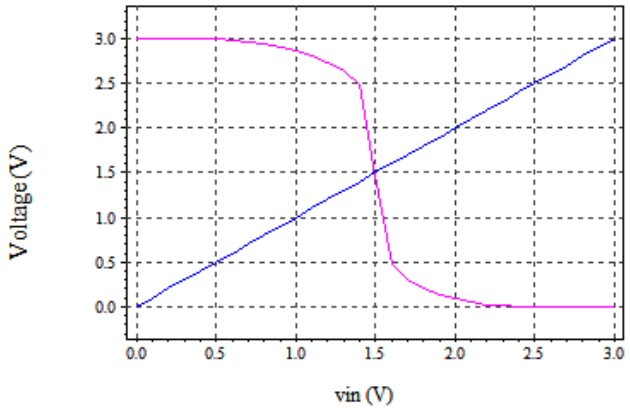



**Fig 2:** I/O characteristics for the chain of inverter based delay line

Fig.2 shows the cut point for the output waveform with respect to the input. This cut point is called the switching threshold voltage at which $V_{in}$= $V_{out}$. This figure shows the switching threshold point for the chain of inverter.

After the analysis we find width of NMOS and PMOS should be 90nm and 220nm respectively and length will be fixed according to the technology node we used. Here we are using 45nm technology node in which 45nm shows the channel length of the transistor. As the length should be 45nm fixed.

## 3. Proposed Delay Line

In this article, delay line is made by connecting even number of inverter in series form. The figure.3 shows the basic block diagram of inverter based delay line.

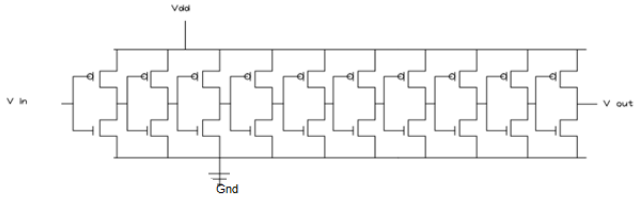



**Fig 3:** Inverter based delay line

The basic structure consists of 10 inverter which are connected in series form. Initially all the inverters are in the steady state. The input V in given to an inverted a supply voltage of 1volt. The delay line is designed with H-Spice 45nm technology.

## 4. Propagation Delay

The propagation delay time ζphl and ζplh determines the input to output signal delay during the high to low and low to high transitions of the output, respectively. Here ζphl is the time delay between the V50% transition of the rising input voltage and the V50% transition of the falling output voltage. Similarly ζplh is the time delay between the V50% transition of the falling input voltage and the V50% transition of the rising output voltage.

The average propagation delay ζp of the inverter characterizes the average time required for the input signal to propagate through the inverter.

$$\tau_p = \frac{\tau_{phl} + \tau_{plh}}{2}$$

Here we analyze the performance parameter of inverter based delay line by varying the supply voltage (0.5 to 1.5). The performance parameter of delay line are leakage current, leakage power and the delay produced by this combination by using H-Spice technology.

## 5. Result and Simulation

### a) Leakage power

Static Power dissipation is the power, when the device is in the ideal mode when there is no input given to the circuit, then there is leakage of power through ground. This power is dissipated from supply voltage to ground. If the supply voltage is more in amount then amount in static or leakage power is more and if voltage is less then leakage power is less. Table.1 shows the variation in leakage power with increase in supply voltage and schematic simulation is plotted in fig 4

**Table 1:** Shows the variation in leakage power with supply voltage.

| Vdd (volts) | Leakage power (watts) |
|---|---|
| 0.5 | 39.5354n |
| 0.6 | 159.6819n |
| 0.7 | 610.1487n |
| 0.8 | 2.1422u |
| 0.9 | 6.5856u |
| 1.0 | 15.2806u |
| 1.1 | 29.7481u |
| 1.2 | 50.1998u |
| 1.3 | 77.8722u |
| 1.4 | 114.6099 |
| 1.5 | 162.8443u |

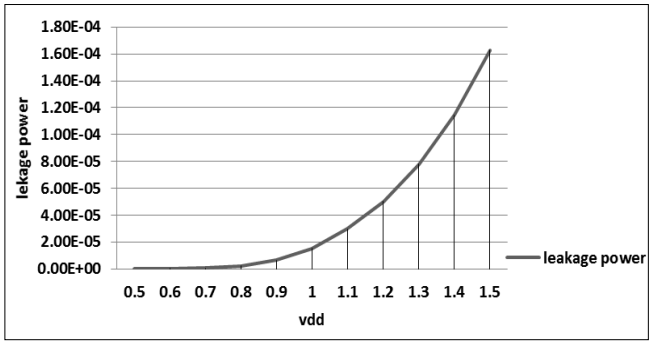



**Fig 4:** Schematic simulation of leakage power with supply voltage.

### b) Leakage current

Table.2 shows the variation in leakage current with supply voltage. And fig. 5 shows the changes in leakage current with supply voltage. The leakage current is also increase with supply voltage.

**Table 2:** Shows the variation in leakage current with supply voltage

| VDD (volts) | Leakage current (amp.) |
|---|---|
| 0.5 | -79.0708n |
| 0.6 | -266.1365n |
| 0.7 | -871.6410n |
| 0.8 | -2.6778u |
| 0.9 | -7.09514u |
| 1.0 | -15.2806u |
| 1.1 | -27.0437u |
| 1.2 | -41.8332u |
| 1.3 | -59.9017u |
| 1.4 | -81.8642u |
| 1.5 | -108.5628u |

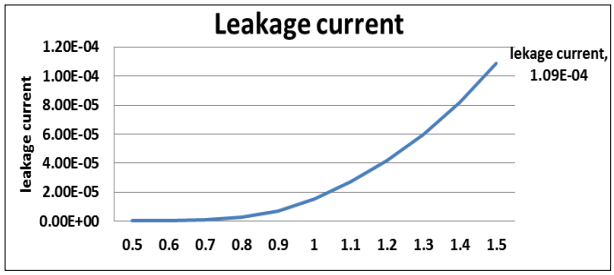



**Fig 5:** Schematic simulation of leakage current with supply voltage.

### c) Propagation Delay

The delay is the time required by a circuit to propagate a signal to generate an output. The delay of the circuit is increase with increase in supply voltage. Table.3 shows the variation in delay time with respect to the supply voltage and fig.6 shows the variation in delay time with supply voltage of the circuit.

**Table 3:** shows the variation in delay time with supply voltage.

| Vdd (volts) | Delay |
|---|---|
| 0.5 | 4.5737E-10 |
| 0.6 | 1.8026E-10 |
| 0.7 | 1.1275E-10 |
| 0.8 | 8.1502E-11 |
| 0.9 | 6.4063E-11 |
| 1.0 | 5.2643E-11 |
| 1.1 | 4.4598E-11 |
| 1.2 | 3.8913E-11 |
| 1.3 | 3.5746E-11 |
| 1.4 | 3.2446E-11 |
| 1.5 | 3.0057E-11 |

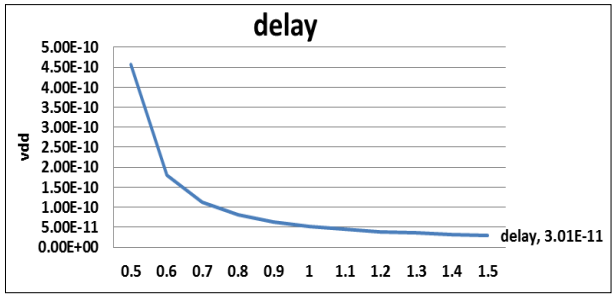



**Fig 6:** Schematic simulation of delay

### d) Power Delay Product

The power delay product is a figure of merit correlated with the energy efficiency. It is also known as the switching energy. It is the product of power consumption (average over a switching event) times the input output delay or duration of the switching event. Table.4 shows the variation in power delay product with supply voltage and fig. 7 shows the variation in power delay product with respect to the supply voltage.

**Table 4:** Power delay product

| VDD | PDP |
|---|---|
| 0.5 | 1.8082E-17 |
| 0.6 | 2.8861E-17 |
| 0.7 | 6.8794E-17 |
| 0.8 | 1.7459E-16 |
| 0.9 | 4.2189E-16 |
| 1.0 | 8.0442E-16 |
| 1.1 | 1.3267E-15 |
| 1.2 | 1.9534E-15 |
| 1.3 | 2.7836E-15 |
| 1.4 | 3.7186E-15 |
| 1.5 | 4.8946E-15 |

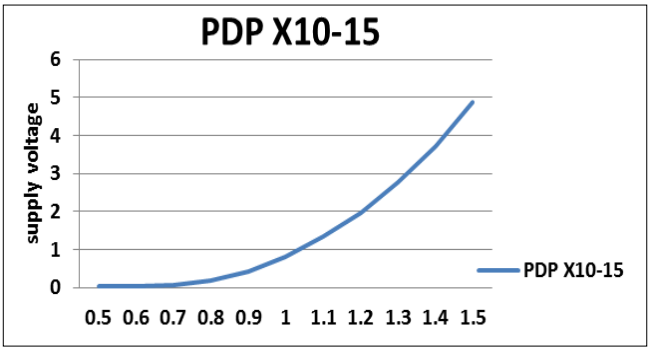



**Fig 7:** Variation in PDP

## 6. Conclusion

Due to tremendous growth in computer and television market, development of great delay line occur. As per increasing requirement, the complexity in delay line also increasing in terms of handling the performance parameter like propagation delay, leakage current, leakage power and PDP. So designer have to control all this performance parameters and these performance parameters and the trend of condition occurring among these parameters.

If we further scaling the technology that we are used then it is possible to get some much better results. This is the only way which can help us for further improving the performance of delay lines.

## 7. References

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